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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,192	11/10/2003	Henry S. Chao	42P17266	5572

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Michael A. Bernadicou
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,192	CHAO ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-17* is/are allowed.

6)☒ Claim(s) *1-10 and 18-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-9, 18, 19, 21 and 23-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Goodwin et al (2004/0043592 A1).

1. Regarding claim 1, Goodwin et al discloses a method comprising: forming a logic gate stack in a logic region (Figure 9, reference 250) on a substrate (Figure 9, reference 202); forming a flash memory gate stack in a flash region (Figure 9, reference 240) on the substrate (Figure 9, reference 202); depositing a hardmask layer over the logic gate stack and over the flash memory gate stack (Figure 8, reference 218; pg.4, paragraph 0044); patterning the hardmask in the logic region so that areas of hardmask remain where logic gates are desired (pg.4, paragraph 0044-0045); patterning the flash gate stack in the flash region to form flash memory gates (pg.4, paragraph 0044-0045); and etching the logic gate stack using the remaining hardmask as a mask to form logic gates (pg.4, paragraph 0045-0047).

2. Regarding claim 2, Goodwin et al discloses wherein the logic region and the flash region are located on a single die (Figure 9, reference 202).

3. Regarding claim 3, Goodwin et al discloses wherein the logic gate stack is comprised of a gate dielectric layer (Figure 9, reference 204) and a gate electrode layer (Figure 9, reference 206).

4. Regarding claim 5, Goodwin et al discloses removing the hardmask layer (pg.4, paragraphs 0044-0045).

5. Regarding claim 6, Goodwin et al discloses wherein the hardmask layer consists of an anti-reflective coating (ARC) hardmask layer (Figure 8, reference 218; pg.4, paragraph 0044).

6. Regarding claim 7, Goodwin et al discloses wherein the ARC hardmask layer is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon (pg.4, claim 3; *organic polymer*).

7. Regarding claim 8, Goodwin et al discloses wherein the ARC hardmask layer is sufficiently damaged by the final logic gate stack etch that it may be easily removed (pg.3, paragraph 0032).

8. Regarding claim 9, Goodwin et al discloses depositing a masking layer over the flash region after patterning the flash gate stack and before etching the logic gate stack to form logic gates (Figure 11, reference 227).

9. Regarding claim 18, Goodwin et al discloses an apparatus comprising: a substrate (Figure 8, reference 202), the substrate having a logic region (Figure 9, reference 250) and a flash region (Figure 9, reference 240); a logic gate stack formed on the substrate in the logic region, the logic gate stack having a top surface (Figure 9, reference 250); regions of antireflective coating (ARC) formed on the top surface of the logic gate stack, the regions of

ARC covering the areas of the logic gate stack where logic gates are to be formed (Figure 8, reference 218); a plurality of flash memory gates formed on the substrate, the flash memory gates having a top surface (Figure 9, references 230a, 230b, and 240); and a layer of resist, wherein the resist covers at least the top surface of the logic gate stack, the regions of ARC formed on top of the logic gate stack, and the top surface of the flash memory gates (Figure 8, reference 220).

10. Regarding claim 19, Goodwin et al discloses wherein the logic gate stack is comprised of a gate dielectric layer (Figure 9, reference 204) and a gate electrode layer (Figure 9, reference 206).

11. Regarding claim 21, Goodwin et al discloses wherein the ARC hardmask layer is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon (pg.4, claim 3; *organic polymer*).

12. Regarding claim 23, Goodwin et al discloses a method comprising: forming a first stack in a first region (Figure 8, reference 250) on a substrate (Figure 8, reference 202) and a second stack in a second region (Figure 8, reference 240) on the substrate (Figure 8, reference 202), wherein the second stack is thicker than the first stack (Figure 9); depositing a hardmask layer over the first stack and the second stack (Figure 8, reference 218); patterning the first region to remove portions of hardmask in the first region (pg.4, paragraph 0044); patterning the second region to remove portions of the hardmask in the second region and portions of the second stack to form the desired geometries of the second stack (pg.4, paragraphs 0044-0045); and removing portions of the first stack using the remaining portions of hardmask as a mask to form the desired geometries of the first stack (pg.4, paragraphs 0044-0048).

13. Regarding claim 24, Goodwin et al discloses a method comprising: forming a logic gate stack in a logic region (Figure 9, reference 250) on a substrate (Figure 9, reference 202); forming a flash memory gate stack in a flash region (Figure 9, reference 240) on the substrate (Figure 9, reference 202); depositing a hardmask layer over the logic gate stack and over the flash memory gate stack (Figure 8, reference 218); patterning the hardmask in the logic region so that areas of hardmask remain where logic gates are desired (pg.4, paragraph 0044); patterning the flash gate stack in the flash region and etching away the hardmask layer and a portion of the flash memory gate stack in the flash region to form a partial flash memory gate (pg.4, paragraphs 0044-0045); and etching the logic gate stack and the remainder of the flash memory gate stack using the remaining hardmask as a mask to form logic gates and flash memory gates (pg.4, paragraph 0045).

14. Regarding claim 25, Goodwin et al discloses wherein the logic region and the flash region are located on a single die (Figure 9, reference 202)

15. Regarding claim 26, Goodwin et al discloses wherein the hardmask layer comprises an antireflective coating (ARC) hardmask layer (Figure 8, reference 218).

16. Regarding claim 27, Goodwin et al discloses wherein the ARC hardmask layer is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon (pg.4, claim 3; *organic polymer*).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodwin et al (2004/0043592 A1) in view of applicant's admitted prior art.

17. Goodwin et al discloses a gate dielectric layer (Figure 9, reference 204) and a control gate electrode layer (Figure 9, reference 208) however, Goodwin et al does not disclose the floating gate layer and inter electrode dielectric layer.

Applicant's admitted prior art discloses the floating gate layer and inter electrode dielectric layer.

It is obvious, at the time the invention was made, for one with ordinary skill in the art, to modify Goodwin et al with the teachings of the applicant's admitted prior art for the purpose of fabricating high density flash memory transistors.

Claims 10, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodwin et al (2004/0043592 A1).

18. Goodwin et al discloses flash memory gates (Figure 9, references 230a, 230b, and 240) and the logic gate (Figure 9, reference 250) however, Goodwin et al does not disclose the specified length and pitch.

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, provide a flash memory gate having a length of less than 150nm and a pitch of

less than 400 and a logic gate having a length of less than 150 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the "optimum range" involves only routine skill in the art. ***In re Aller***, 105 USPQ 233 (1955).

Allowable Subject Matter

19. Claims 11-17 are allowed over the prior art of record.

Reasons for Allowance

20. The following is an examiner's statement of reasons for allowance: The primary reason for allowance of the claims is that the prior art neither teaches nor fairly suggest a method for fabricating a logic gate stack and a flash memory stack on a substrate as presented in claims 11-17 and in the context of the recited process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is 571-272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Monica D. Harrison
AU 2813

mdh
June 8, 2005

CRAIG A. THOMPSON
PRIMARY EXAMINER